

# Modeling and Simulation of Differential Voltage Controlled Current Source (DVCCS) for Artificial Neural Networks (ANNs) Applications

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**Abstract**— We proposed a mixed analog/digital VLSI system for convolutional neural networks using digital circuit technique. Verification of successful operation of all circuit components were done using HSPICE program. This paper presents modeling and simulation for the Differential Voltage Controlled Current Source (DVCCS) designed in 0.34  $\mu\text{m}$  CMOS technology which is CMOS wideband transconductance amplifier. The output current during capabilities as well as the frequency response have been simulated using Monte Carlo analysis in order to investigate the effect of dispersion in process parameters. The control over the amplifier bandwidth is obtained by adequate design of the main biasing current. The transfer characteristic curve non linearity is also studied.

**Keywords:** Differential Voltage current control SUPER MOSFET, Artificial Neural Network.

## I. INTRODUCTION

A VLSI neural network can be applied in many applications requiring fast, low power operations. Modeling and circuit design a small synapse with one D/A per weight can be achieved by a binary weighted current source and then feeding the binary weighted currents into diode connected transistors on the synapse to convert them back to currents. Thus we achieve many D/A's with only one binary weighted away of transistor. The role is being determined by which side of the current mirror acts as a very simple analog neuron whose output terminal is tied to one of the summing nodes.

One of the most promising approaches for implementing Artificial Neural Networks ANNs is through the use of electronic analog/ digital VLSI circuits because ANNs attempts to behave similarly to the brain with its millions of neurons. VLSI is the most appropriate presently available technology for their hardware implementations. Further more, both VLSI circuits and biological neurons are of the same clam that is fundamentally analog. [1-3]

The present VLSI ANNs consist of synaptic weights

implemented by amplifier gains summation of the weighted signals activation functions realized by amplifier nonlinearities and dynamics via capacitor for smoothly transitioning from an initial state to a desired equilibrium. The work horse of analog VLSI ANNs is the Differential Voltage Controlled Current Source (DVCCS) and capacitors. The DVCCS is used for making synaptic weights and activation function and capacitors are used for dynamics [4-5]. A DVCCS takes a voltage difference as input, and gives an output as a function of that difference. DVCCS gains can realize the weights when operating on small signals in a linear region and can also realize saturation nonlinearities when operating on large signals. Using capacitors in conjunction with DVCCS to establish any linear circuit so that any desired filtering of ANNs signals is available, as may be needed in special applications such as ANNs [6-7]. Along with the DVCCS and capacitor, it is also convenient to have resistors for conversion of currents to voltage and voltage divisions, as well as for current sources and current mirrors respectively. Our proposed neuron circuit is shown in figure (1) where the input signals are connected with the non-linear function and weighted summation is performed by converting the signal into charges stored in capacitor  $C_N$ . The voltage of the capacitor is converted into digital signal by comparing it with linearly ramped voltage signal  $V_{ref}$ [8-10]

In section II of this paper Modeling and circuit design is presented, and the proposed DVCCS is presented in section III. Simulations and measurements results are presented in section IV followed by discussion and conclusions in section V.

## II. MODELING AND CIRCUIT DESIGN

### A. Super MOS as a perfect matched current mirror:

The idea of super MOS based on that, the output current  $I_{ds}$  of the MOSFET transistor has a great dependence on the effective channel length in the form of the channel length

modulation parameter ( $\lambda$ ). The output conductance of the small signal model is also proportional to  $1/\lambda$ . It can be shown that the drain current in the saturation region increases slightly in a linear manner with  $V_{ds}$ . This is physically due to a slight shortening of the channel length as  $V_{ds}$  is increased in the saturation region. The channel modulation parameter  $\lambda$  is the coefficient that represents the linear dependence of  $I_{ds}$  on  $V_{ds}$ . The effect of  $\lambda$  is drastically reduced in Super NMOS transistors which means that the Super MOS can also be used in a perfect matched current mirror.

The Super MOS behaves like a cascade MOS transistor having source, gate and drain terminals. Also, the Super NMOS consists of four regular PMOS and eight NMOS. The circuit is self biasing and therefore very easy to use in design, it behaves as a single MOS transistor but with nearly zero channel modulation factor  $\lambda$  and intrinsic gain of more than 90 dB. The Super MOS however has an extremely high output impedance due to implementation of the gain-boosting technique. Moreover, it does not require any biasing voltage or current other than one single power supply. Referring to Figure. 2, transistor  $MN_1$  is the main transistor while  $MN_2$  is its cascade. They form the core of the circuit and their sizes determine the current-voltage relationships and the high frequency behavior of the device. The relation between the threshold voltage of the Super MOS and the dimension of the transistor  $MN_3$  ( $W_3$ ), in particular we assume all transistors are working in saturation region as presented by Alazab and H. F. Ragai in [ 11 ] Moreover, the Super MOS has a high output impedance due to implementation of the gain-boosting technique and needs a single power supply

### B. DVCCS:

The two of the key components in an ANN are the weights and the nonlinear activation function. A weight can be realized by a DVCCS operating in its linear region while a nonlinear activation function can be realized by operating a DVCCS over its full nonlinear range. The transconductance amplifier generates its output as a current that is a function of the difference between two input voltages,  $V_1$  and  $V_2$ . The differential pair is shown in Figure. 3 as an input stage  $mp_1$  and  $mp_2$ . The two transistors  $mp_5$  and  $mp_6$  are used as a current source, under normal circumstances, its drain voltage is larger enough that the drain current  $I_{bias}$  saturated at a value set by the gate voltage  $V_g$ . The manner in which  $I_{bias}$  is divided between  $mp_1$  and  $mp_2$  is a sensitive function of the difference between  $V_1$  and  $V_2$  and is the essence of the operation of the stage

The three current mirrors  $MN_1$ ,  $MN_3$  and  $MN_2$ ,  $MN_4$  beside  $MP_3$  and  $MP_4$  are used to generate output current that is proportional to the difference between the two differential drain currents  $I_1$  and  $I_2$  where the current  $I_1$  drain out of  $MP_1$  is reflected as an equal current out of  $MP_4$  and the current  $I_2$  drawn out of  $MP_2$  is reflected as equal current out of  $MN_4$ . To implement this function we design the circuit in CMOS 0.34

$\mu m$  technology. All transistors work in saturation mode for the specified output current level. The design procedure starts by adjusting the DC potential level at the gate of the bias current source  $MP_6$  and at the output at half the supply voltage with both inputs shorted to ground.

The Differential voltage current controlled source is a device that generates as its output current that is a function of the difference between two input voltages  $V_1$  and  $V_2$ . The differential pair is shown in Figure 2 as an input stage  $MP_1$  and  $MP_2$ . the two transistors  $MP_5$  and  $MP_6$  are used as a current source, under normal circumstances, its drain voltage is large enough that the drain current  $I_{bias}$  is saturated at a value set by the gate voltage  $V_g$ . The manner in which  $I_{bias}$  is divided between  $MP_1$  and  $MP_2$  is a sensitive function of the difference between  $V_1$  and  $V_2$  and is the essence of the operation of the stage.

### C. Analysis

The current mirrors allow current to flow only in one direction. However, by placing a P-mirror on top of an N-mirror . we can get a bi-directional current mirror which is convenient for realizing weights . With the steering controlled by the voltage difference of the input voltages, and the current mirrors. We know that the saturation current is:

$$I = \frac{K_p}{2} (V_{gs} - V_T)^2 \dots\dots\dots(1)$$

where  $K_p$  is a material constant.

Applying this expression to the proposed circuit diagram figure 2 to  $mn_1$  and  $mn_2$  transistors using the current mirror ratio 1:1 we find

$$I_1 = 0.5 I_{bias} \left(1 + \frac{I_{out}}{I_{bias}}\right) \dots\dots\dots(2)$$

And

$$I_2 = 0.5 I_{bias} \left(1 - \frac{I_{out}}{I_{bias}}\right) \dots\dots\dots(3)$$

The sum of the two drain currents must be equal to the bias current

$$I_{bias} = I_1 + I_2 \dots\dots\dots(4)$$

The sum of the two drain currents must be equal to the bias current

$$I_{bias} = I_1 + I_2 \dots\dots\dots(5)$$

then

$$V_{in} = \frac{I_{out}}{\sqrt{K_p I_{bias}}} \dots\dots\dots(6)$$

The transconductance  $G$  of the DVCCS is just the slope of the output current versus the input voltage curve .

$$G = \frac{I_{out}}{V_{in}} = \sqrt{K_p I_{bias}} \dots\dots\dots(7)$$

Notice that the transconductance is proportional to the bias  $I$  bias, a fact that will become important when the amplifier is used to produce a voltage type output

### III. SIMULATION RESULTS

HSPICE has been used to carry out the different types of analysis mentioned above. Figure 4 gives a transfer characteristics with a given bias current which can be seen to have a transconductance (slope) of about 160  $\mu$ S.

The AC analysis is shown in figure 5, which give the same value at low frequency, and is carried out to get the circuit gain and bandwidth which is inherently high in current mode operation. Monte Carlo (MC) analysis is carried out on the DC offset output current. The values of threshold voltage and transconductance parameters can varies widely due to processing spread. The mean offset current is found to be close to the value originally estimated from the typical circuit elements.

The histogram is found to be reasonably sharp. Analysis is carried out by considering the parasitic capacitances of all MOSFET. Junction areas and perimeters are estimated according to the layout design rules for the targeted technology.

### IV. DISCUSSION AND CONCLUSIONS:

In this work a Super MOS whose threshold voltage is mask programmable through changing the dimensions of a single transistor and the simple transconductance DVCCS with wide band operatin and the current capability is sufficiently high for driving capacitive load which is more suitable for implementing the artificial neural networks

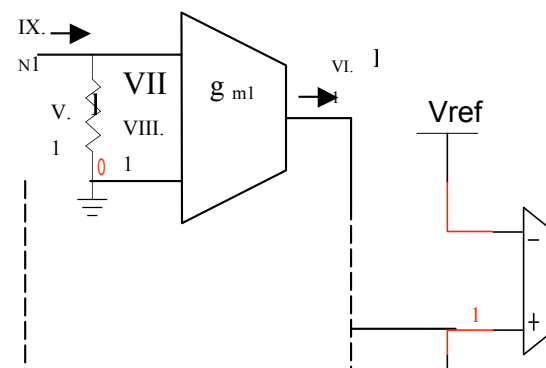
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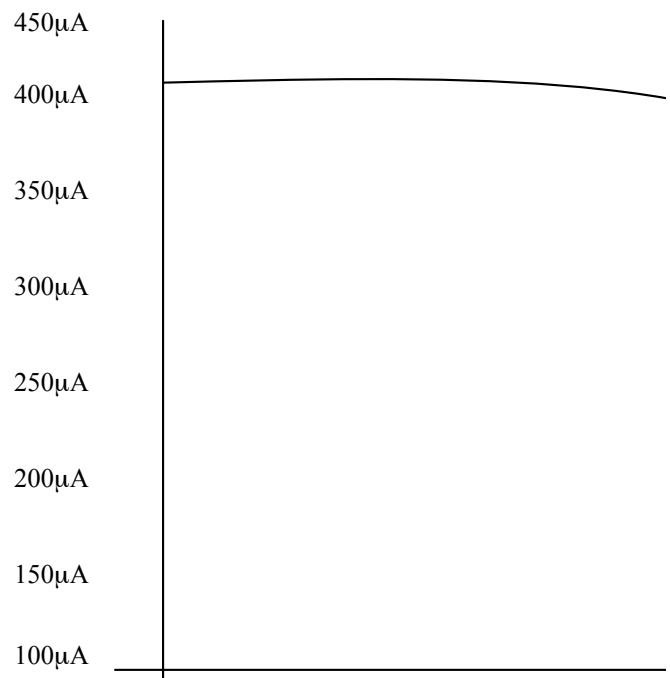
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DC output current



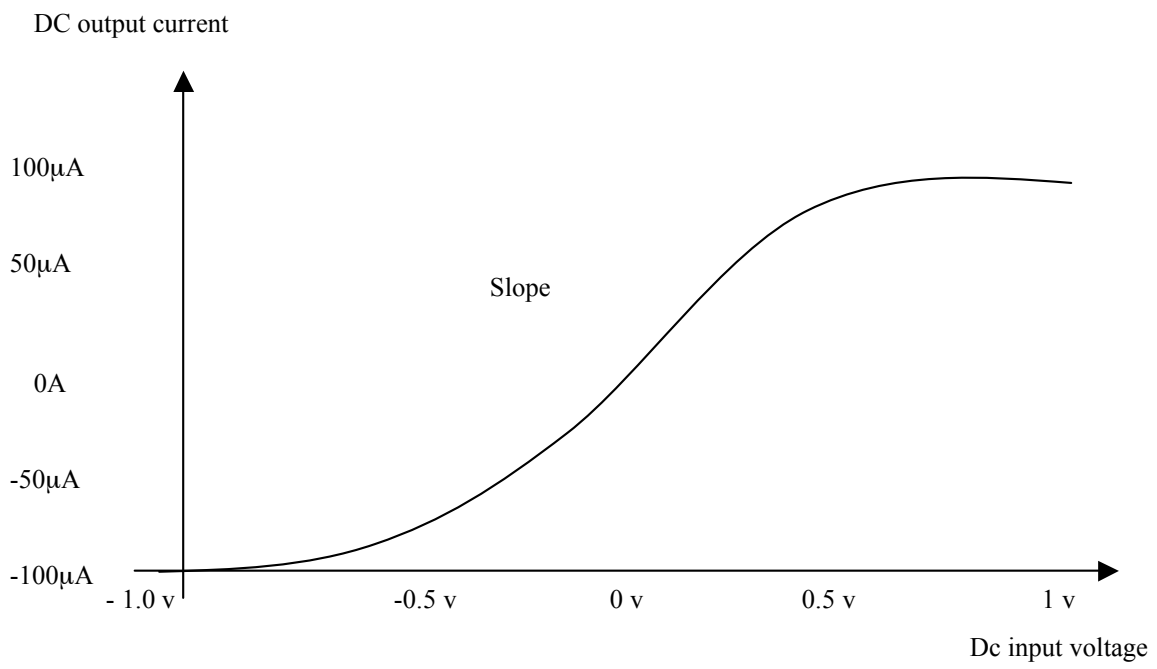


Figure (4) Transfer communication